AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 8, lines 3-28 of the Specification with the following amended paragraph:

Because of the perspective angle used in FIG. 2, the output pad on MMIC 8 for signal 4 cannot be directly seen, but is shown in outline by dashed lines in FIG. 2. The pad for signal 4 is coupled to a high-frequency trace 30 by a respective solder bump 7. Trace 30 conveys electrical signal 4 to coupling structure 20, where it is coupled to patch antenna 24 by way of a conductive via 32. The position of via 32 is outlined by dashed lines in FIGS. 1 and 2, and is shown in cross-sectional view by FIG. 4. FIG. 4 shows ground plane 26 and electrical trace 30 disposed on the top major surface of substrate 1; shows patch antenna 24, capacitive diaphragm 28, ground ring 22, and ground plane 34 disposed on the bottom major surface of substrate 1; and shows a via [[29]] 32 disposed through substrate 1 and electrically coupled to trace 30 and patch 24. Electrical trace 30 is preferably configured as a planar transmission line, and more preferably as a microstrip line or a coplanar waveguide line. Instead of microstrip line or coplanar waveguide line, preferred implementations of trace 30 may be configured as slot-lines, coplanar strips, and symmetrical striplines, as well as other types of planar transmission lines. As is known in the art, a microstrip line comprises a conductive trace disposed on one surface of a substrate layer, and conductive ground plane disposed on the opposite surface of the substrate layer and underlying the conductive trace. A microstrip configuration for the electrical trace 30 is show in FIGS. 1 and 2 where the underlying ground plane is shown at reference number 34 in FIG. 1. A grounded coplanar waveguide line comprises the electrical trace and underlying ground plane of the microstrip structure (*e.g.*, trace 30 and ground plane 34), plus additional ground planes on the top surface of the substrate layer, and disposed on either side of the electrical trace. The additional ground planes are shown in dashed lines at reference numbers 36 and 38 in FIGS. 2 and 3. The additional ground planes 36 and 38 are preferably electrically coupled to the underlying ground plane 34 by a plurality of electrically conductive vias 39. Each location of a via 39 is outlined by dashed circle in FIGS. 1 and 2, and an exemplary one is shown in cross-sectional view by FIG. 3. As seen in FIG. 3 with the reference numbers shown within parentheses, ground planes 34 and 36 are disposed on opposite surfaces of substrate 1,

and via 39 is disposed through substrate 1 and between ground planes 34 and 36. In addition, conductive trace 30 and ground planes 34, 36 and 38 may be formed within substrate layer 1 if substrate layer 1 comprises multiple interleaving sub-layers of dielectric material and patterned conductive material.

Please replace the paragraph at page 6, lines 27-29 of the Specification with the following amended paragraph:

In preferred practice of the present invention, a ground plane 34 is included on bottom major surface 2 of substrate layer 1 to aid in constructing impedance-controlled transmission lines on top major surface 3. As described below in greater detail, preferred embodiments may also include conductive vias **29** for electrically coupling capacitive diaphragm 28 to a ground plane (not shown in FIG. 1) that is hidden behind the diaphragm, and may include conductive vias **39** for electrically coupling ground plane 34 to other ground planes (not shown in FIG. 1) that are hidden behind ground plane 34. Conductive vias **29** and **39** are shown in FIG. 1 by dashed lines.

Please replace the paragraph at page 9, lines 20-29 of the Specification with the following amended paragraph:

As indicated above, patch antenna 24, capacitive diaphragm 28, trace 30, and ground planes 34, 36, and 38 may be formed on patterned conductive sub-layers of substrate layer 1 when substrate layer 1 comprises a plurality of interleaving dielectric and conductive sub-layers. In such a case, these components are positioned within substrate layer 1 and between bottom major surface 2 and top major surface 3. In addition, a dielectric sub-layer may be laminated onto top major surface 3 and ground plane 26, and additional conductive and dielectric sub-layers may be laminated onto the first laminated dielectric sub-layer, if desired. It may be appreciated that in such a case, for the purposes of the claims of the application, the substrate layer 1 comprises the sub-layers between ground ring 22 and ground plane 26. An example of substrate layer 1 comprising sub-layers is illustrated in FIG. 8, where substrate layer 1 comprises three dielectric sub-layers disposed between bottom major surface 2 and top major surface 3. Patch antenna 24 and capacitive diaphragm 28 are disposed between the two lower

dielectric sub-layers of substrate layer 1, whereas trace 30 is disposed between the two upper dielectric sub-layers of substrate layer 1. As in prior embodiments, conductive via 32 provides an electrical connection between patch antenna 24 and electrical trace 30; ground plane 26 is disposed on top major substrate 3; and ground plane 34 is disposed on bottom major substrate 2. Ground ring 22 is disposed at bottom major surface 2, and is electrically coupled to ground plane 34 and capacitive diaphragm 28.